NATIONAL INSTITUTE OF TECHNOLOGY, ARUNACHAL PRADESH
(Established by MHRD, Govt. of India)
YUPIA, ARUNACHAL PRADESH -791112, INDIA

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Advt. No.: ECE/P/AM/02/2019/DST(SERB)/ Date: 06-03-2023

The interview for the temporary post of 'Junior Research Fellow (JRF)' **under SERB CRG Project (No. CRG/2019/006362) titled "**Integration of Variable Frequency Clock and Gated Clock Tree to Mitigate Power Supply Noise in Multi-core CPU**" will be conducted in the** Dept. of Electronics & Communication Engineering (ECE), NIT Arunachal Pradesh on **15th March 2023 (Wednesday) via GOOGLE MEET** at 11:00 AM onwards.

1	Name of the Post	Junior Research Fellow (JRF) - 01
2	Name of the Research Project	Integration of Variable Frequency Clock and Gated Clock Tree to Mitigate Power Supply Noise in Multi-core CPU
3	Name of the Sponsoring Agency	SERB (Govt. of India)
4	Tenure of the Project	Till Completion of the project or 05-08-2023
5	Tenure of the Assignment	Not Extendable
6	Job Description	One **JRF** is required for the study of Power Supply Noise (PSN) mitigation techniques in Multi-core CPU / Silicon ICs. The final goal is to devise a novel circuital technique to curb down PSN.
7	Consolidated monthly compensation / Fellowship	Rs. 31,000/- per month+ (HRA as per Norms)
8	Essential Qualifications and experience	BE/B-Tech in ECE/EE/CSE/EEE with Valid Gate Score and ME / M.Tech in VLSI/ Microelectronics/Nanotechnology/Power Electronics and related areas with Gate. Knowledge in VLSI design tools (Cadence, Mentor Graphics) are desirable
9	Accommodation	Bachelors Accommodation in the Institute Hostel may be provided subject to availability

Eligible candidates may appear for the online interview at the Department of Electronics & Communication Engineering, National Institute of Technology Arunachal Pradesh. The candidates are advised to send a mail to alak.icas@gmail.com on or before **12th March 2023** ***(5.00 PM)*** with a subject "***Application for JRF position in the project no. CRG/2019/006362***" along with the relevant documents: CV, mark sheets, research papers (if any) and experience certificate (if any) etc. attached in a single PDF. The link of GOOGLE MEET will be shared to the candidates prior to the date/time of interview. Mere possession of essential/desirable qualification and experience does not guarantee selection for the post. Candidates will be selected on merit and need of the project.

Dean (R & D)
NIT Arunachal Pradesh
Yupia

संकायाध्यक्ष/Dean
अनुसंधान एवं परामर्श/Research and Consultancy
राष्ट्रीय प्रौद्योगिकी संस्थान/National Institute of Technology
अरुणाचल प्रदेश/Arunachal Pradesh Jote-791113

Copy to:
1. All Heads of the Departments, NIT Arunachal Pradesh for publication on Departmental Notice Boards.
2. Dr. Alak Majumder, PI with a request to give wide publicity of the advertisement.
3. Head of the Department, Electronics & Communication Engineering
4. Project file