National Institute of Technology

(Established by Ministry of Education, Shiksha Mantralaya Govt. of India)

Yupia, District: Papum Pare, Arunachal Pradesh 791112

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ADVERTISEMENT NO.: .ECE/AM/JRF/0I (RE-ADVERTTSEMENT) **DATED: 09.02.2021**

Project No.: **ECE/P/AM/02/2019/DST(SERB)/**
Sanction No.: **CRG/2019/006362**

The interview for the temporary post of 'Junior Research Fellow (JRF)' **under SERB CRG Project (No. CRG/2019/006362) entitled** "Integration of Variable Frequency Clock and Gated Clock Tree to Mitigate Power Supply Noise in Multi-core CPU" **will be conducted in the** Dept. of Electronics & Communication Engineering (ECE), NIT Arunachal Pradesh on **22th February 2021 via GOOGLE MEET** at 10:30 AM

1	Name of the Post	Junior Research Fellow (JRF) - 01
2	Name of the Research Project	Integration of Variable Frequency Clock and Gated Clock Tree to Mitigate Power Supply Noise in Multi-core CPU
3	Name of the Sponsoring Agency	SERB (Govt. of India)
4	Tenure of the Project	03 Years
5	Tenure of the Assignment	Extendable annually till completion of project subject to the satisfactory performance and availability of fund released by sponsoring agency
6	Job Description	**JRF** is required for the study of Power Supply Noise (PSN) mitigation techniques in Multi-core CPU / Silicon ICs. The final goal is to devise a novel circuital technique to curb down PSN.
7	Consolidated monthly compensation / Fellowship	Rs. 31,000/- per month + HRA (as per norms)
8	Essential Qualifications and experience	BE (ECE/EE/EIE/EEE) and ME / M.Tech in VLSI / Microelectronics / Nanotechnology / Electronic System and related areas. Candidate must have qualified GATE during his / her academic career. Knowledge is VLSI design tools (Cadence, Mentor Graphics) is desirable.
9	Accommodation	Bachelors Accommodation in the Institute Hostel may be provided, subject to availability.

Eligible candidates may appear for the online interview at the Department of Electronics & Communication Engineering, National Institute of Technology Arunachal Pradesh. The candidates are advised to send a mail to alak@nitap.ac.in on or before ***18th Feb' 2021 (5.00 PM)*** with a subject

P.K.M
9/2/2021.

"***Application for JRF position in the project no. CRG/2019/006362***" along with the relevant documents: CV, mark sheets, research papers (if any) and experience certificate (if any) etc. attached in a single PDF. The link of GOOGLE MEET will be shared to the candidates prior to the date of interview. Mere possession of essential/desirable qualification and experience does not guarantee selection for the post. Candidates will be selected on merit and need of the project.

09/02/2021.

DIC (R & D)
NIT Arunachal Pradesh

डीन (आर एंड डी)/Dean (R & D)
राष्ट्रीय प्रौद्योगिकी संस्थान, अरूणाचल प्रदेश
National Institute of Technology, Arunachal Pradesh
Yupia, Arunachal Pradesh-791112, India

Copy to:

1. All Heads of the Departments, NIT Arunachal Pradesh for publication on Departmental Notice Boards.
2. Dr. Alak Majumder, PI with a request to give wide publicity of the advertisement.
3. Head of the Department, Electronics & Communication Engineering
4. Project file