NATIONAL INSTITUTE OF TECHNOLOGY ARUNACHAL PRADESH
(Established by Ministry of Human Resources Development, Govt. Of India)
Yupia, District Papum Pare, Arunachal Pradesh – 791112
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Department of Electronics & Communication Engineering

M.Tech. in VLSI & Embedded Systems (2019 Onwards)

Semester - 1

Code	Subject	L	T	P	Credit
MAS XXX	Mathematics	3	0	0	3
ECE 501	Physics of Semiconductor Devices	3	0	0	3
ECE 502	Digital CMOS IC	3	0	0	3
ECE 503	Analog IC Design	3	0	0	3
ECE 504	Embedded Systems &IoT	3	0	0	3
ECE 505	VLSI Lab I	0	0	8	4
ECE 506	Embedded Systems Design Lab I	0	0	4	2
					21

Semester - 2

Code	Subject	L	T	P	Credit
ECE5 07	Mixed Signal IC Design	3	0	0	3
ECE XXX	Elective I	3	0	0	3
ECE XXX	Elective II	3	0	0	3
ECE XXX	Elective III	3	0	0	3
ECE 508	VLSI Lab II	0	0	4	2
ECE 509	Embedded Systems Design Lab - II	0	0	8	4
					18

Semester - 3

Code	Subject	L	T	P	Credit
ECE 598	M-Tech Thesis Preliminary	-	-	-	10
					10

Semester - 4

Code	Subject	L	T	P	Cr
ECE 599	M-Tech Thesis Final	-	-	-	16
					16

List of Electives

Code	Subject	L	T	P	Credit
ECE 521	MEMS & Microsystem	3	0	0	3
ECE 522	Memory Design & Testing	3	0	0	3
ECE523	Embedded Systems for Industrial Automation	3	0	0	3
ECE 524	CAD for VLSI	3	0	0	3
ECE525	RF IC Design	3	0	0	3
ECE 526	Testing &Verification	3	0	0	3

ECE 527	VLSI System Design	3	0	0	3
ECE 528	VLSI DSP Architectures	3	0	0	3
ECE 529	Advanced DSP Processors	3	0	0	3
ECE 530	Pattern Recognition & Machine Learning	3	0	0	3
ECE 531	Wireless Communication	3	0	0	3

Physics of Semiconductor Devices

Unit-I

***Semiconductor fundamentals*:** Band theory, E-k diagram, Effective mass, Density of states, Statistics, Carrier density, Degeneracy, Compensation.

***Transport*:** Ohm's law, Mobility, Boltzmann equation, Hall mobility, Diffusion, Scattering mechanisms, Hot electrons.

***Excess carriers*:** Recombination in direct gap, SRH theory, Traps, Continuity equation.

***P-N Junction theory*:** Band diagram of semiconductor P-N junction, Depletion width, Built-in potential, I-V characteristics, Varactor diode.

Unit–II

***Bipolar junction transistors*:** Minority carrier distribution and terminal currents, Generalized biasing, Switching, Secondary effects, Frequency limitations of transistors.

***MOS Capacitors and MOSFETs*:** Band diagram under depletion, Inversion and accumulation, Threshold voltage and its control, C-V curves, I-V characteristics, Gradual channel approximation, Charge sheet model, Pao-Sah current formulation, Subthreshold current conduction, Channel length modulation, Hot electrons.

Unit-III

***Advanced MOSFETs*:** CMOS scaling, Short channel effects, Threshold voltage roll-off, DIBL, GIDL, Gate leakage current, Hot carrier injection, Punch through, Silicon-on-insulators (SOI) MOSFETs, Low Power and high speed design issues.

Unit–IV

***Heterostructures and Quantum Well Devices*:** Quantization and low dimensional electron gas, Influence on MOSFET characteristics, Band alignment in Si/SiGe heterostructures, High electron mobility transistors (HEMTs), Quantum Well FETs, FinFET, FDSOI.

Text and Reference Books:

1. B. G. Streetman and S. K. Banerjee, "Solid State Electronic Devices", 6/e, PHI Private Limited, 2011.
2. P. Bhattacharya, "Semiconductor Optoelectronic Devices", 2/e, PHI, 2009.
3. G. Massobrio and P. Antognetti, "Semiconductor Device Modeling with SPICE", 2/e, TMH, 2010.
4. C. C. Hu, "Modern Semiconductor Devices for Integrated Circuits", Pearson Education, 2010.
5. R. S. Muller and T. I. Kamins, "Device Electronics for Integrated Circuits", 3/e, Wiley India, 2009.
6. S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices", 3/e, Wiley India, 2010.
7. Y. Tsividis, "Operation and Modeling of the MOS transistor", 2/e, TMH, 1999.
8. D. A. Neamen and D. Biswas, "Semiconductor Physics and Devices", 4/e, TMH, 2012.

Digital CMOS IC

Unit-I

MOS transistor theory**:** Ideal I-V Characteristics, C-V Characteristics, Non-ideal I-V Effects, DC transfer characteristics.

Electrical wire models**:** The ideal wire, The lumped model, The lumped RC model and The distributed RC line.

The CMOS inverter**:** The static CMOS inverter, The static behaviour- Switching threshold, Noise margin, The dynamic behaviour- Computing capacitances, Propagation delay, Power, Energy and Energy Delay - Dynamic, Static and Short circuit, Technology scaling and its impact.

CMOS fabrication and layout**:** Fabrication process, Layout design rules - stick diagram, Technology related CAD issues, Manufacturing issues, Custom to semicustom and structured array design approaches, Cell based design methodology, Array based implementation approaches.

Unit–II

Designing CMOS combinational logic gates**:** Static CMOS design - complimentary CMOS, Ratioed logic and pass transistor logic, Dynamic CMOS design - dynamic logic, speed and power dissipation, Signal integrity issues, Designing logic for reduced supply voltages.

Designing sequential logic circuits**:** Timing metrics, Static latches and registers - bistability principle, Multiplexer based latches, Master-Slave edge triggered register, Low voltage static latches, Dynamic latches and registers, Pipelining, Synchronous design- Timing basics, Sources of skew and jitter, Clock distribution approaches.

Unit–III

Interconnects**:** Capacitive parasitics – crosstalk, capacitance and performance in CMOS, Resistive parasitics – resistance and reliability, Electromigration and RC delay, Inductive parasitics, Reduced swing circuits.

Arithmetic and logic circuits**:** Adder circuits – carry look-ahead adder, Carry select adder, Multipliers; Barrel shifters, General purpose functional blocks and ALU design.

Unit–IV

Low power circuits**:** Leakage in CMOS nanometric technologies, Modelling for designing in deep submicron technologies, Low power dynamic logic circuits, Circuit techniques for dynamic power reduction, Circuit techniques for leakage reduction, adiabatic and clock powered circuits.

Text and reference Books:

1. J.M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuits- A Design Perspective", 2/e, PHI, 2003
2. S.M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", 3/d, McGraw Hill, 2003
3. J. P. Uyemura, "Introduction to VLSI Circuits and Systems", Springer, 2014
4. David A. Hodges, Horace G. Jackson and R. A. Saleh, "Analysis and Design of Digital Integrated Circuits in Deep Submicron Technologies", 3/e, McGraw-Hill, 2003.

Analog IC Design

Unit–I

***Review of MOS transistor*:** MOSFET structure, MOS I-V characteristics, Second order effects, MOS device models.
***Single stage amplifiers*:** Common source, Source follower, Common gate, Cascode.
***Analog CMOS sub-circuits*:** MOS switch, Current sink and sources, Current mirrors, Current and voltage references.

Unit-II

***Differential amplifiers*:** Single ended and differential, Basic differential pair; Common mode response, Gilbert cell.
***Frequency response of amplifiers*:** Miller effect, Common source stage, Source followers, Common gate, Cascode stage, Differential pair.

Unit–III

***Noise*:** Characteristics, types and representation, Noise in single stage and differential amplifiers.
***Feedback*:** Properties of feedback circuits, Types, Feedback topologies, Effect of loading.
***Oscillators*:** General Consideration, Ring oscillators; LC oscillators, Voltage Controlled Oscillators.

Unit–IV

***Operational amplifiers*:** Basic concepts, Performance parameters, One stage Op-amp, Two stage Op-amp, Gain boosting, Slew rate, Power supply rejection ratio, Stability and frequency compensation.
***High performance CMOS Op-amps*:** Micropower Op-amps, Low noise Op-amps, Low voltage Op-amps.
***Comparators*:** Characterization, Two stage open loop comparator, Other open loop comparators, Improving the performance of open loop comparators.

Text and Reference Books:

1. B. Razavi, "Design of Analog CMOS Integrated Circuits", 2/e, McGraw Hill, 2017.
2. Gray, Hurst, Lewis and Meyer, "Analysis and Design of Analog Integrated Circuits", 5/e, Wiley, 2009.
3. Adel Sedra and Kenneth C. Smith, "Microelectronic Circuits", 7/e, Oxford University Press, 2017.
4. R. Jacob Baker, Harry W. Li and David E. Boyce, "CMOS: Circuit Design, Layout, and Simulation", 1/e, Wiley, 2009.
5. T. C. Carusone, D. Johns and K. Martin, "Analog Integrated Circuit Design", 2/e, Wiley, 2013.
6. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", 3/e, Oxford University Press, 2013.

Embedded Systems & IoT

Unit-I

Review of Embedded system: Requirements of embedded system, Hardware software co-design, architecture, challenges and design issues in embedded systems.
Review: of 8051 and PIC, design consideration and applications.

Unit-II

Advance Microcontroller: ARM- Introduction to ARM processor and ARM processor family, architecture and advance functionality of ARM and programming techniques, exception handling, case study, Raspberry Pi- Architecture and advance functionality of the latest Raspberry Pi, programming techniques, exception handling, case study.
Advanced Arduino processor: Architecture and advanced functionality of the Arduino and Intel Galileo, programming techniques, exception handling, case study.
FPGA based embedded system: Programmable interconnect; partitioning and placement routing resources, delays, Dynamic architecture using FPGAs, reconfigurable systems, arbiter design, application case studies.

Unit-III

RTOS: Tasks, process and threads, Multi-processing and multi-tasking, Task scheduling, Inter process communication, message passing, interrupt driven input and output – non-maskable interrupt, software interrupt. Threads – single, multi-thread concept; multitasking sequential circuit, task synchronization techniques. Handling of interrupts in RTOS and timing analysis.
Application: Implementation of advance embedded controller for actuator and sensor interfacing, high end application in the field of robotics.

Unit-IV

IoT: Introduction to IoT Platform, Data management, Artificial intelligence application in IoT, cloud computing, IoT Security, IoT device energy level issues. Interfacing a sensor and Appliances control through server; Design challenges.

Text and Reference Books:

1. Muhammad Ali Mazidi, Janice Gillispie Mazidi and Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C",2/e, Pearson, 2007.
2. Muhammad Ali Mazidi, Sarmad Naimi and Sepehr Naimi, "AVR Microcontroller and Embedded Systems", 1/e, Pearson, 2012.
3. Andrew Robinson and Mike Cook, "Raspberry Pi Projects", 1/e, Wiley, 2014.
4. Arockia Bazil Raj, "FPGA-Based Embedded System Developer's Guide", 1/e, CRC Press, 2018.
5. Cuno Pfister, Getting Started with the Internet of Things: Connecting Sensors and Microcontrollers to the Cloud (Make: Projects)", 1/e, Shroff, 2011.

VLSI Lab I

1. Standard Cell design of static CMOS based inverter, buffer, NAND gate and NOR gate for equal rise, fall time around a load of 1pF.
2. Standard Cell design of conventional Master-Slave configured D Latch and D Flip-Flop.
3. Standard Cell design of Transmission-Gate (TG), TG based Multiplexer and De-multiplexer for equal rise, fall time around a load of 1pF.
4. Standard Cell design of 1 bit digital comparator, priority Encoder/Decoder and Adder/Subtractor around a load of 1pF.
5. Design & Analysis of a ring oscillator and VCO.
6. Design of a 4 bit memory (comprising of bit cell and row/column decoder).

Embedded Systems Design Lab I

1. To study Proteus design suit, Arduino and Galileo: Blinking LED, Driving RGB LED, Driving multiple LEDs, Driving relays using push button, Driving a motor using timer and interrupt, Reading a sensor data and store in memory and resend to a target port.
   2 links 2 DoF joint controller design-
   I. Planning
   II. Algorithm development
   III. Simulation
   IV. Implementation and verification

2. To study Experiments using Raspberry Pi: Python tutorial and practices, IoT Smart garage door opener using Raspberry Pi, Real Time Face Recognition using Raspberry Pi and Opencv.
3. FPGA based embedded system design: Simulation and Implementation, Writing a basic software application to access peripherals devices, adding a timer and interrupt controller generate periodic events, Arbiter design for sensors and actuators interfacing-
   I. Planning
   II. Algorithm development
   III. Simulation
   IV. Implementation and verification

Mixed Signal IC Design

Unit–I

***Switched capacitor circuits*:** Switched capacitor amplifiers, Switched capacitor integrators, z domain models of two phase switched capacitor circuits, 1^{st} and 2^{nd} order switched capacitor circuits, Switched capacitor filters.

Unit–II

***Analog filter design*:** Bilinear transfer functions and frequency, cascade design with 1^{st} order circuits, The biquad circuit, Butterworth lowpass filters, Butterworth bandpass filters, The Chebyshev response, Frequency transformations, Highpass and band elimination filters, Ladder design, Leapfrog simulation of ladders.

Unit-III

Phase locked loops: Revision of VCOs, Simple PLL, Charge pump PLLs, Nonideal effects in PLLs; Delay locked loops, Applications.

Unit–IV

***Data converter fundamentals*:** Ideal D/A converters, Ideal A/D converter; Serial and Flash D/A converters and A/D converters, Medium and High Speed converters, Over-sampling converters, Performance limitations, Design consideration.

Text and Reference Books:

1. B. Razavi, "Design of Analog CMOS Integrated Circuits", 2/e, McGraw Hill, 2017.
2. Gray, Hurst, Lewis and Meyer, "Analysis and Design of Analog Integrated Circuits", 5/e, Wiley, 2009.
3. Adel Sedra and Kenneth C. Smith, "Microelectronic Circuits", 7/e, Oxford University Press, 2017.
4. R. Jacob Baker, Harry W. Li and David E. Boyce, "CMOS: Circuit Design, Layout, and Simulation", 1/e, Wiley, 2009.
5. T. C. Carusone, D. Johns and K. Martin, "Analog Integrated Circuit Design", 2/e, Wiley, 2013.
6. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", 3/e, Oxford University Press, 2013.

VLSI Lab II

1. Characterization of NMOS & PMOS Transistor (both DC and AC) and Analysis of current equation.
2. Standard Cell design of a Common Source / Common Gate / Common Drain Amplifier for different loads (like 50fF, 500fF and 1pF).
3. Standard Cell design of a Single stage Cascode Amplifier for different loads (like 50fF, 500fF and 1pF).
4. Standard Cell design of a Current Mirror along with Differential Pair for different loads (like 50fF, 500fF and 1pF).
5. Design of a single and two-stage Op-Amp with different loads (like 50fF, 500fF and 1pF).
6. Design and Analysis of an ideal PLL circuit.

Embedded Systems Design Lab II

1. To study distributed embedded system using Proteus design suit.
2. Robot multiple link joint controller for industrial automation.
3. ARM based embedded system design using μKeil simulator and implementation using ARM .
4. Demonstrate ARM Cortex-M Programming using μKeil and debugging using Unilink LED pattern design using input/output ports.
5. To study timing analysis using logic analyzer for automatic material handling system.
6. To study the embedded security for embedded system.
7. To study embedded system development techniques using Matlab.
8. To study embedded system development techniques using Labview.

Electives

MEMS & Microsystem

Unit–I

***Overview of MEMS and Microsystems*:** Introduction, Evolution of MEMS, Microfabrication, Typical MEMS, Microsystems products and their applications, Introduction to smart materials and systems.

Unit–II

***Working principles of MEMS and Microsystems*:** Introduction to microsensors and microactuators, Electrical and mechanical concepts in MEMS, Sensing techniques for MEMS piezoresistive, Piezoelectric, Capacitive and Optical sensing methods, Piezoresistive sensor materials, piezoelectric materials, Applications for tactile, flow, inertia and pressure sensors, Microactuation techniques for MEMS: Actuation methods using thermal forces, piezoelectric crystals and electrostatic forces, Examples of MEMS based microsensors and microactuators.

Unit-III

***Microsystems materials*:** Substrates and wafers, active substrate materials, Gallium Arsenide, Quartz, piezoelectric crystals.

***Fabrication processes*:** Silicon wafer processing, Thin film deposition, Photolithography, Diffusion, Ion Implantation, Oxidation, Chemical Vapor Deposition, Physical vapor deposition – Sputtering, Deposition by Epitaxy, Etching Techniques, packaging materials.

***Micromachining processes*:** Bulk Micromachining and Surface Micromachining, the LIGA Process, other moulding techniques, Introduction to soft lithography and thick film processing, Overview of polymers in MEMS, MEMS for RF Applications.

Unit–IV

***Electronic circuits for MEMS and Microsystems Semiconductor devices*:** Interface electronics for MEMS, Overview of Diodes, BJT, MOSFET, CMOS, Electronic amplifiers, Operational amplifiers, Differential amplifiers, Wheatstone Bridge circuits for measurement of resistance and analog to digital converters for MEMS and Microsystems, Signal conditioning for Microsystems devices, Differential charge measurement, switched capacitor circuits for capacitance measurement, Control and Microsystems, Smart sensors and MEMS, MEMS Simulators.

Text and Reference Books:

1. T. R. Hsu, "MEMS and Microsystems Design and Manufacture", 1/e, Tata McGraw-Hill, 2017.
2. S. D. Senturia, "Microsystem Design", 1/e, Springer, 2003.
3. M. J. Madou, "Fundamentals of Microfabrication: The Science of Miniaturization", 2/e, CRC Press, 2018.
4. C. Liu, "Foundations of MEMS", Pearson, 2011.
5. N. Maluf, "An Introduction to Microelectromechanical Systems Engineering", 2/e, Artech House, 2000.
6. J. W. Gardner, "Microsensors: Principles and Applications", Wiley, 1994.

Memory Design & Testing

Unit–I

***Static RAM*:** Cell design – CMOS NAND and NOR memory cells, Read/Write operation, SRAM cell layout, Address decoders – Row and column decoders, Sense amplifiers.

Memory array organization: Memory address and address decoders, row and column decoders, access time management, sense amplifiers, Single and multiport memories, Cache memories.

Unit–II

***Dynamic RAM*:** Three-transistor cell, one-transistor cell, external characteristics of dynamic RAM

***Read-only Memories* (*ROM*):** Review of basic MOS physics – Threshold voltage and its control, EPROM, EEPROM, Flash memory, FRAMs; MOS ROM Cell arrays.

Unit–III

***Content Addressable Memories*:** BCAM, TCAM.

***Advanced Topics*:** Magnetic memory cells - Giant Magneto-resistance phenomenon, MRAM, ReRAM, spintronics.

Unit–IV

***Memory Modeling and testing faults in SRAMs*:** Open, short, bridge fault, Delay faults. Functional fault modeling and testing of SRAMs, Test for single cell and two port SRAMs, Marching Tests, Fault diagnosis & Repair algorithms, Built – in self test and design for testability of RAMs, Built in self repair architecture, Trend in embedded memory testing.

Text and Reference Books:

1. J.M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuits- A Design Perspective", 2/e, PHI, 2003.
2. R. Jacob Baker, Harry W. Li, David E. Boyce, "CMOS: Circuit Design, Layout, and Simulation", 2/e, Pearson, 2016.
3. A. K. Sharma, "Semiconductor Memories: Technology, Testing and Reliability", Wiley-Blackwell, 2002.
4. C. Hu, "Nonvolatile Semiconductor Memories: Technologies, Design and Applications", 1/e, IEEE, 1991.
5. K. Itoh, "VLSI Memory Chip Design", Springer, 2001.
6. G. Sun, "Exploring Memory Hierarchy Design with Emerging Memory Technologies", Springer, 2013.
7. C. Shin, "Variation Aware Advanced CMOS Devices and SRAM", 1/e, Springer, 2016.

Embedded Systems for Industrial Automation

Unit-I

***Introduction*:** Embedded systems, Applications in industrial automation, Networked systems design. ***System modeling*:** System specification, Hardware/software: partitioning problem, Cost estimation, Co-design, System specification and modeling.

***RTOS*:** Task scheduling, Handling of interrupts and timing analysis.

Unit-II

***Drives controller for industrial automation*:** Pneumatic drives, Hydraulic drives, Mechanical drives, electrical drive d.c. Servo motors, a.c., Servo motors features, Stepper motor, Applications and comparison of drives.

***End effectors controllers for Industrial Automation*:** Mechanical grippers, Magnetic grippers, Vacuum grippers, Two fingered and three fingered grippers, Internal grippers and external grippers.

Unit-III

***Sensors for Industrial Automation*:** Sensors for motion, vision, sonar, Joint movement etc. commonly used in industrial automation.

***Design Consideration for Embedded Circuit*:** I/O interfacing with different drives, sensors using different advanced microcontroller.

Unit-IV

***Basics of Automation*:** Co-ordinate systems, Work envelope, Pitch, Yaw, Roll, Joint notations, Forward kinematics, Inverse kinematics of manipulators controller for two, Three degrees of freedom.

***Embedded Controller Design Implementation*:** Optimization and implementation techniques using suitable embedded controller (Raspberry PI, Arduino, etc.) and FPGA.

Text and Reference Books:

1. Myke Predko, "Programming and Customizing the 8051 Microcontroller", McGraw-Hill International, 1999.
2. J. W. Stewart and J. J. Mistovich, "The 8051Microcontroller: Hardware, Software and Interfacing", 2/e, 1998.
3. M. P. Groover, M. Weiss and R. Nagel, "Industrial Robotics – Technology, Programming and Applications", McGraw-Hill, 1987.
4. K.S. Fu, C. S. George Lee and Ralph Gonzalez., "Robotics Control, Sensing, Vision and Intelligence", McGraw, 1987.
5. Yoram Koren, "Robotics for Engineers", McGraw-Hill, 1985.

CAD for VLSI

Unit-I

***Matrices*:** Linear dependence of vectors, Solution of linear equations, Bases of vector spaces, orthogonality, Complementary orthogonal spaces and solution spaces of linear equations.

***Graphs*:** Representation of graphs using matrices, Paths, Connectedness, Circuits, Cutsets, Trees, Fundamentals circuit and cutset matrices, Voltage and current spaces of a directed graph and their complementary orthogonality.

Unit-II

***Algorithms and data structures*:** Efficient representation of graphs, Elementary graph algorithms involving BFS and DFS trees, Such as finding connected and 2-connected components of a graph, The minimum spanning tree, Shortest path between a pair of vertices in a graph.

Unit-III

Algorithms for VLSI physical design, Synthesis, Circuit simulation and digital design automation.

Unit-IV

Algorithms for design automation using FPGA/CPLD, Fault tolerant systems, VLSI testing.

Text and Reference Books:

1. K. Hoffman and R.A. Kunze, "Linear Algebra", Prentice Hall, 1986.
2. N. Balabanian and T.A. Bickart, "Linear Network Theory; Analysis, Properties, Design and Synthesis", Matrix Publishers, Inc., 1981.
3. T. H. Cormen, C. E. Leiserson and R.L. Rivest, "Introduction to Algorithms", MIT press and McGraw Hill, 1990.
4. N. Shervani, "Algorithms for VLSI Physical Design Automation", 3/e, Kluwer Academic Publishers, 1998
5. W. J. McCalla, "Fundamentals of Computer-Aided Circuit Simulation", Kluwer Academic Publishers, 1987
6. G. De Micheli, "Synthesis and Optimization of Digital Circuits", Tata McGraw Hill, 2003.
7. S. H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 1999.

RF IC Design

Unit–I

***Introduction*: ** Basics of RF systems, Review of circuit theory- impedance concept, reflection and maximum power transfer.

***Tuned Circuits*:** Series and parallel RLC networks, Q-factor, matching

***RF IC components*:** Resistance, capacitance and inductance, skin effect; Review of MOS transistor.

Unit–II

***Transmission Lines*:** The wave equation and its solutions, reflections, lossy transmission lines, Smith chart and its use.

***RF Amplifiers*:** Amplifier topologies, bandwidth estimation, rise-time, delay and bandwidth, Shunt-series amplifiers, Cascaded amplifiers.

***Power amplifiers*:** Class A, B, AB and C amplifiers, Switching power amplifiers, RF power amplifier design examples.

Unit–III

***Noise*:** Signal and noise, Noise sources – thermal noise, flicker noise; noise figure, Intrinsic MOS noise parameters, Power match vs noise match, Low noise amplifier concept.

***Oscillators*:** Oscillator topologies, RF Resonators, Negative resistance oscillators.

Unit–IV

***Mixers*:** Multiplier based mixers, large signal performance, Design examples.

***Phase Locked Loops*:** Linearized PLL Models; Phase detectors, charge pumps, loop filters; CMOS VCO, PLL Design examples.

***Frequency Synthesis*:** Frequency dividers and multipliers, Frequency synthesizer examples.

***Radio architectures*:** GSM, CDMA and UMTS system architectures.

Text and Reference Books:

1. Thomas H. Lee, "The Design of CMOS Radio Frequency Integrated Circuits", 2/e, Cambridge University Press, 2004.
2. Behzad Razavi, "RF Microelectronics", 2/e, Pearson, 2013.

Test & Verification

Unit-I

Course introduction, VLSI design flow, Need of pre-silicon verification and post-silicon validation and debug, VLSI testing needs and challenges, Test challenges, Yield, and Defects, Faults and fault models, Yield and fault equivalence.

Unit-II

Combinational equivalence checking, BDD operations and SAT, Logic simulation, Fault simulation, Deductive and concurrent fault simulation, Combinational equivalence checking, Automatic test pattern generation (ATPG): algebraic method.

Unit-III

D algorithm, PODEM, PODEM, FAN, Sequential equivalence checking, Sequential ATPG, Sequential equivalence checking, Sequential equivalence checking, Scan design, Sequential equivalence checking.

Unit-IV

Model checking, Issues in san design, Random access scan, Random access scan, Basics of model checking, Partial scan, LTL,LTL & CTL.

Text and Reference Books:

1. M. L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits", Springer, 2009.
2. H. Fujiwara, "Logic Testing and Design for Testability", MIT Press, 1985.
3. M. Abramovici, M. Breuer, and A. Friedman, "Digital System Testing and Testable Design", 1/e, Jaico Publishing House, 2001.
4. M. Huth and M. Ryan, "Logic in Computer Science- Modelling and Reasoning about Systems", 2/e, Cambridge Univ. Press, 2005.
5. T. Kropf, "Introduction to Formal Hardware Verification", 1/e, Springer, 2010.

VLSI System Design

Unit- I

***Basics of system hardware design*:** Hierarchical design using top-down and bottom-up methodology, System partitioning techniques, Interfacing between system components.

***Programmable Logic Devices*:** FPGA, CPLD, PLA, PAL.

***Design Phases*:** Design, Testing, Fabrication, Packaging, Abstraction and their Types.

***Computer Aided Designs*:** Modeling & simulation, VLSI design flow, ASIC design flow.

Unit-II

***Designing basic building blocks*:** Digital systems design using conventional components such as gates, flip flops, PALs, and FPGAs etc.

***Synchronous and Asynchronous Circuits*:** Concept of finite state machine (FSM), Moor and Mealy machines, synchronous FSM Design, State diagram, State assignment, Derivation of next state and Output expressions, Arithmetic logic design, Designing multi data path ALU, Algorithmic state machine.

***Memories*:** Introduction to different types of memories, Single and multiple port memories.

Introduction to GALS (Globally Asynchronous Locally Synchronous).

***Introduction to Network on Chip*.**

***Introduction to FIFO and designing fast FIFOs*.**

Unit-III

***Clocks*:** Static timing analysis; Handling multiple clock domains, Global and local clock distribution, Case studies involving system designing using CAD tools around soft-core processors and other peripherals (I/O, Memories etc.).

Unit- IV

***Processor Design*:** Von Neumann architecture, Harvard architecture, Modified Harvard architecture.

***Datapath and Control*:** Enhancing performance with pipelining, Exploiting memory hierarchy.

***Case studies using Intel X86 family of Advanced Microprocessors*:** Programming model for x86 family.

***8086 Microprocessor Architecture*:** Addressing modes, Instruction set, Assembly language programming; Stacks, Micros, Interrupts, Interrupt service routines, 8086 system bus structure.

***I/O Programming*. *Multiprocessor Configurations*:** Coprocessors.

***Memory and I/O Interfacing*:** Parallel and serial communication interface, D/A and A/D interface, Timers.

***Keyboard/display controller*:** Interrupt controller, DMA controller.

***Hardware of 186, 286, 386, 486 & Pentium processors*.**

Text Books:

1. M. Morris Mano, "Digital Logic & Computer Design", 1/e, Pearson, 2016.
2. D. A. Patterson and J. L. Hennessy, "Computer Organization and Design: The Hardware/Software Interface", 2/e, Morgan Kaufmann Publishers Inc., 1998.
3. J. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuits - A Design Perspective", 2/e, Pearson Education, 2011.

VLSI DSP Architectures

Unit-I

***Introduction to digital signal processing systems*:** Typical DSP algorithms, DSP application demands and scaled CMOS technologies, Representations of DSP algorithms.

***Iteration bound*:** Data flow graph representation, Loop bound and iteration bound, Algorithms for computing iteration bound, Iteration bound of multirate data flow graphs.

***Pipelining and parallel processing*:** Pipelining of FIR digital filters, Parallel processing, Pipelining and parallel processing for low power.

Unit-II

***Retiming*:** Definition and properties, Solving system of equalities, Retiming techniques.

***Unfolding*:** Algorithm for unfolding, Properties of unfolding, Critical path, Unfolding and retiming, Applications.

***Folding*:** Folding transformation, Register minimization techniques, Register minimization in folded architectures, Folding of multirate systems.

***Systolic architecture design*:** Systolic array design methodology, FIR systolic arrays, Selection of scheduling vector, Systolic design for space representations containing delays.

Unit-III

***Fast convolution*:** Cook Toom, Winograd and Iterated algorithm, Cyclic Convolution.

***Algorithmic strength reduction in filters and transforms*:** Parallel FIR filters, DCT and inverse DCT, Parallel architectures for rank order filters.

***Pipelined and parallel recursive and adaptive filters*:** Pipeline interleaving in digital filters, Pipelining in 1^{st} order IIR digital filters, Pipelining in high order IIR digital filters, Parallel processing for IIR filters, Low power IIR filter design using pipelining and parallel processing, Pipelined adaptive digital filters.

Unit-IV

Scaling and round off noise: State variable description of digital filters, Scaling and roundoff noise computation, Roundoff noise in pipelined IIR filters, Roundoff noise computation using state variable description.

***Digital Lattice Filter Structures*:** Digital basic lattice filters, Derivation of one multiplier, Normalized, Scaled normalized lattice filter, Roundoff noise calculation, Pipelining of lattice IIR digital filter.

***Bit Level Arithmetic Architectures*:** Parallel multipliers, Bit serial multipliers, Bit serial filter design, Distributed arithmetic.

***Redundant Arithmetic*:** Subexpression elimination, Multiple constant multiplication, Additive and multiplicative number splitting.

Text and References Books

1. K. K. Parhi, "VLSI Digital Signal Processing and Systems, Design and Implementation", John Wiley, 1999.
2. U. Meyer Baese, "Digital Signal Processing with FPGA", 3/e, Springer, 2007.
3. S. Ramachandran, "Digital VLSI Systems Design", Springer 2007
4. K. Madisetti, "VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis", IEEE Press 1995.

Pattern Recognition & Machine Learning

Unit-I

Introduction: Problem framing, feature selection, Dimensionality reduction using PCA and other methods.

Discriminative classifiers: LDA, Multi-layer perceptron, Backpropagation, SVM.

Unit-II

Unsupervised learning: Clustering, Vector quantization, Kohonen map, EM algorithm, ***Generative models***: Definition and characteristics, probabilistic graphical models, density estimation in learning.

Unit-III

Combining classifiers: Advantages, Boosting, Hierarchical classifiers and issues, Selected special topics such as manifold learning and case studies.

Text and Reference Books:

1. S. Marsland, "Machine Learning: An Algorithmic Perspective", 2/e, Chapman & Hall/CRC, 2014.
2. R. O. Duda, P. E. Hart and D. G. Stork, "Pattern Classification", 2/e., Wiley, 2007.
3. C. M. Bishop, "Pattern Recognition and Machine Learning (Information Science and Statistics)", 1/e, Springer, 2006.
4. I. H. Witten, "Data Mining: Practical Machine Learning Tools And Techniques", 3/e, Elsevier, 2014.

Wireless Communication

Unit-I

Overview of current wireless systems and standards;

Wireless channel models: path loss and shadowing models; statistical fading models; narrowband and wideband fading models; MIMO channels.

Unit-II

Diversity in wireless communications - Non-coherent and coherent reception; error probability for uncoded transmission; realization of diversity: time diversity; frequency diversity: DSSS and OFDM; receiver diversity: SC, EGC and MRC; transmit diversity: space-time codes;

Unit-III

Information theory for wireless communications- Capacity of fading channels: ergodic capacity and outage capacity; high versus low SNR regime; waterfilling algorithm; capacity of MIMO channels;

Unit-IV

Multiuser wireless communications: multiple access: FDMA, TDMA, CDMA and SDMA schemes; interference management: power control; multiuser diversity, multiuser MIMO systems.

Texts & Reference Books:

1. A. J. Goldsmith, *Wireless Communications*, Cambridge University Press, 2005.
2. D. Tse and P. Viswanath, *Fundamentals of Wireless Communication*, Cambridge University Press, 2005.
3. A. Molisch, *Wireless Communications*, John Wiley & Sons, 2005.
4. S. Haykin and M. Moher, *Modern Wireless Communications*, Pearson Education, 2005.
5. T. S. Rappaport, *Wireless Communications*, Prentice Hall, 1996.
6. G. L. Stuber, *Principles of Mobile Communications*, Kluwer, 1996.
7. T. Cover and J. Thomas, *Elements of Information Theory*, John Wiley & Sons, 1991.